Introduction to Printed Circuit Board Design For EMC Compliance

Mark Montrose
Principle Consultant
Montrose Compliance Services, Inc.
+ 1 (408) 247-5715
mark@montrosecompliance.com
www.montrosecompliance.com
Fundamentals of Signal Integrity
**What is Signal Integrity**

The ability of electrical signals to travel from a source to load through a dielectric without loss of signal amplitude or parametric values.

In order to solve a signal integrity problem, one must first understand transmission lines and how they function both in theory and reality.

*There are two kinds of design engineers:
“Those that have signal integrity problems, and those that will”*
## Signal Integrity Concerns

It only takes **one** item listed below to cause a signal integrity problem

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<td>High dielectric losses</td>
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Aspects of High-Speed Problems

Four aspects of high-speed problems are present in system designs

1. **Signal quality**: Reflections and distortions from impedance discontinuities in the signal or return path can affect the quality of the signal. A transmitted signal should see the same impedance throughout all interconnects (includes vias and connectors).

2. **Crosstalk between nets**: Mutual capacitance and inductance exists, both within an ideal and non-ideal return path. One must keep spacing of traces greater than a minimal value while minimizing mutual inductance, keeping the return path impedance as low as possible.

3. **Rail collapse**: A voltage drop within the power and return system when digital components switch logic states. One must minimize the impedance of the power and return path along with the delta-I (current).

4. **EMI**: Can be developed as a result of poor signal integrity within a transmission line. Must minimize bandwidth, ground impedance and common-mode coupling.

Details on impedance discontinuities, transmission line routing, terminations, and simulations are presented later.
**Lossless Transmission Line Equivalent Circuit Within a PCB**

![Diagram of a lossless transmission line equivalent circuit within a PCB](image)

\[
Z_0 = \sqrt{\frac{L_0}{C_0}} = \frac{V(x)}{I(x)} \quad \text{and} \quad t_{pd} = \sqrt{\frac{L_{total}}{C_{total}}}
\]

Lossy Transmission Line Equivalent Circuit Within a PCB

\[ V(\omega, x) = V_0 \exp(-\Gamma x) \exp(jt) \]
\[ \Gamma = \alpha + j\beta = \sqrt{(RL + j\omega LL) + (GL + j\omega CL)} \]
\[ Z_0 = \frac{(RL + j\omega LL)}{\sqrt{(GL + j\omega CL)}} \]

\[ Z_0 = \text{characteristic impedance} \]
\[ L = \text{line length} \]
\[ RL, GL \text{ may vary with frequency} \]
**Lossy Transmission Lines**

1. **Resistive losses** - Constant with frequency. Attenuation, usually measured in dB/unit distance, is proportional to the resistance per unit length of the conductor.

2. **Skin effect losses** - Proportional to the square root of frequency. As signal frequency increases, current flow retreats to the surface of the conductor flowing in a "skin" which becomes thinner with increasing frequency. Resistivity of the material stays the same, it is the cross section that decreases related to AC current flow.

3. **Dielectric losses** - The PCB material (core and prepreg) absorbs some of the electric field energy, which is directly proportional to frequency. Dielectric loss or dissipation factor (magnitude of energy loss) is not the same as dielectric constant (speed of signal travel).

4. **Resonances** - Typically caused by improperly terminated traces and split planes in addition to the lumped magnitude of both capacitance and inductance within power distribution networks.
Typical Transmission Line System

- Minimum reflections will occur when $Z_{out} = Z_o$ and $Z_o = Z_{load}$
- Maximum energy transfer occurs when $Z_{out} = Z_o = Z_{load}$

If the load is not matched, a voltage is reflected back toward the source. The value of reflected voltage ($V_r$) and the percentage of the propagation signal reflected back towards the source (%) is:

$$V_r = V_o \left( \frac{R_{Load} - Z_o}{R_{Load} + Z_o} \right) \quad \text{and} \quad \text{% reflection} = \left( \frac{Z_L - Z_o}{Z_L + Z_o} \right) \times 100$$

where $V_r$ = reflected voltage
$V_o$ = source voltage
$R_L$ = load resistance
$Z_o$ = characteristic impedance of the transmission path

When $R_L$ is less than $Z_o$, a negative reflected wave exist. If $R_L$ is greater than $Z_o$, a positive wave is observed. This reflected wave will bounce back and forth between source and driver until dielectric losses absorbs the signal.

<table>
<thead>
<tr>
<th>Cable Type</th>
<th>Characteristic Impedance</th>
</tr>
</thead>
<tbody>
<tr>
<td>RG174</td>
<td>50 Ω</td>
</tr>
<tr>
<td>RG58</td>
<td>50 Ω</td>
</tr>
<tr>
<td>RG59</td>
<td>75 Ω</td>
</tr>
<tr>
<td>RG62</td>
<td>93 Ω</td>
</tr>
<tr>
<td>TV Antenna</td>
<td>300 Ω</td>
</tr>
<tr>
<td>Cable TV</td>
<td>75 Ω</td>
</tr>
<tr>
<td>Twisted pairs</td>
<td>70-120 Ω</td>
</tr>
</tbody>
</table>
Reflections – Poor Signal Integrity

Reflections will occur within a transmission line if not properly terminated. The following causes reflections.

- Changes in trace width
- Improperly matched termination networks
- Lack of terminations
- T-stubs, branched or bifurcated traces
- Varying loads and logic families
- Connector transitions
- Any changes in impedance of the transmission line routing

Ringing indicates excessive capacitance

Rounding indicates excessive inductance
Crosstalk – Fundamental Aspects of Coupling

\[ Z_v = \frac{Z_s(v) \times Z_L(v)}{Z_s(v) + Z_L(v)} \]

- \( Z_s \) (source) and \( Z_s \) (victim) are impedances associated with the source and victim traces, respectively.
- \( C_{sv} \) is the capacitance between the source trace and the victim trace.
- \( C_{vg} \) is the capacitance between the victim trace and ground.
- \( C_{sg} \) is the capacitance between the source trace and ground.

Inductive coupling is illustrated by the inductance \( L_m \) between the traces.

Ground plane or reference structure.
Schematic representation of a three wire circuit

\[ C_{sv} = \text{Capacitance between source trace and victim trace} \]
\[ C_{vg} = \text{Capacitance between victim trace and ground} \]
\[ C_{sg} = \text{Capacitance between source trace and ground} \]
8.0 inches (20.3 cm) long, 72.1 ohms
Propagational delay: 1.126 ns
Oscillator: 66 MHz, 49% duty cycle
CMOS, 3.3V, Fast
Traces: 0.008" wide and 0.008" apart (.20mm)
Distance to reference plane: 0.010" (.25mm)
Common Forms of Crosstalk

Far End Cross Talk
Only appears in surface traces and scales with coupling length, inversely with rise time and depends on line to line spacing. Reduce it by shorter coupling lengths, longer rise time, larger spacing, or best of all, route in stripline.

Near End Cross Talk
Saturates with coupling length when coupling TD > ½ RT (rise time), predominantly affected by line to line spacing and can be reduced with lower dielectric constant.
Sample List of Design Techniques to Prevent Crosstalk

To prevent crosstalk within a PCB, the following design and layout techniques are useful.

- Crosstalk will increase with a wider trace width as mutual capacitance, $C_m$, increases.
- With long parallel traces, greater mutual inductance, $L_m$, is present.
- Crosstalk also increases with faster edge rates and frequency of operation.

1. Group logic devices according to functionality.
2. Minimize routed distance between components.
3. Minimize parallel routed trace lengths.
4. Locate components away from I/O interconnects and areas susceptible to field corruption.
5. Provide terminations for traces rich in harmonic energy.
6. Avoid routing of traces parallel to each other with adequate separation between the tracks.
7. Route adjacent signal layers (either microstrip or stripline) orthogonally to prevent capacitive and inductive coupling between two planes in parallel.
8. Reduce signal-to-ground reference distance separation.
9. Reduce trace impedance and/or signal drive level.
10. Isolate signal layers routed in the same axis by a solid planar (typical of backplane designs).
**Power and/or Return Plane Bounce**

\[ V_{\text{power/return}} = L_{\text{power/return}} \frac{dI}{d\text{discharge}} \]

![Diagram of power and/or return plane bounce](image)
Fundamentals of EMC
### Component Characteristics at RF Frequencies

(The Hidden Schematic)

<table>
<thead>
<tr>
<th>COMPONENT</th>
<th>LOW FREQUENCY BEHAVIOR</th>
<th>HIGH FREQUENCY BEHAVIOR (Lumped version)</th>
<th>RESPONSE</th>
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</thead>
<tbody>
<tr>
<td>WIRE</td>
<td></td>
<td></td>
<td>$Z$</td>
</tr>
<tr>
<td>RESISTOR</td>
<td></td>
<td></td>
<td>$Z$</td>
</tr>
<tr>
<td>INDUCTOR</td>
<td></td>
<td></td>
<td>$Z$</td>
</tr>
<tr>
<td>CAPACITOR</td>
<td></td>
<td></td>
<td>$Z$</td>
</tr>
<tr>
<td>TRANSFORMER</td>
<td></td>
<td></td>
<td>$Z$</td>
</tr>
</tbody>
</table>

**Response curves**
- Solid line is low frequency behavior
- Dashed line is high frequency behavior

**How RF Energy is Created – Maxwell Made Simple**

Maxwell’s four equations describe the relationship of electric and magnetic fields. Equations are derived from:

- Ampere’s Law
- Faraday’s Law
- Two from Gauss’s Law.

**To overly simplify Maxwell, use Ohms law**

**Ohms Law (time domain-DC currents)**

\[ V = I \times R \]

**Ohms Law (frequency domain-AC currents)**

\[ V_{rf} = I_{rf} \times Z \]
Right Hand Rule
(Faraday’s Law)

Field or Flux Line
(Magnetic Flux)

I (Current in the wire)

Where is the electric field? In the direction of current flow.
Only the magnetic field is shown as a flux line.
Maxwell's Equations
(For Reference Purposes)

First Law : Electric Flux (from Gauss)
\[ \nabla \cdot D = \rho \quad \varphi_e = \int_s D \cdot ds = \int_v \rho \, dv = 0 \]

Second Law : Magnetic Flux (from Gauss)
\[ \nabla \cdot B = 0 \quad \varphi_m = \int_s B \cdot ds = 0 \]

Third Law : Electric Potential (from Faraday)
\[ \nabla \times E = -\frac{\partial B}{\partial t} \quad \oint E \cdot dl = -\int_s \frac{\partial B}{\partial t} \cdot ds \]

Fourth Law : Electric Current (from Ampere)
\[ \nabla \times H = J + \frac{\partial D}{\partial t} \quad \oint H \cdot dl = \int_s \left( J + \frac{\partial D}{\partial t} \right) \cdot ds = I_{total} \]
A plane wave is a combination of both electric and magnetic field components (Poynting vector). Fields propagate from a field source near the velocity of light.

\[ c = \frac{1}{\sqrt{\mu_0 \varepsilon_0}} = 3 \times 10^8 \]

where \( \mu_0 = 4\pi \times 10^{-7} \) H/m
\( \varepsilon_0 = 8.85 \times 10^{-12} \) F/m

Electric field component is measured in volts/meter (Note-voltage)
Magnetic field component is in amps/meter (Note-current)

The ratio of both electric field (E) to magnetic field (H) is identified as the "impedance" of free space. This impedance ratio is described by:

\[ Z_0 = E \times H = \sqrt{\frac{\mu_0}{\varepsilon_0}} = 377 \text{ ohms} \] (Note-resistance)

Energy carried in the wave front is measured in Watts/meter\(^2\) (Note-power)
Electric and Magnetic Field Representation

Dipole Antenna

Loop Antenna
If a continuous, conductive low impedance RF return path is not present (transmission line impedance is greater than 377 ohms), the return path will be free space (377 Ω at λ/4), which may be much less than the impedance of a localized RF return path.
Radiated Emissions from a Closed Loop Circuit

This configuration is for a single- or double-sided PCB. For a multi-layer PCB, loop area is in the plane directly below the signal path.
Loop Area Between Circuits or Components – Different Layers

The real loop area is longer than shown, as the transmission line must have both a source and return path. Only the source path is shown. The return path is through either the power or ground plane, depending on application.
Return Current Path of Travel – Multilayer Assembly

Low frequency operation

High frequency operation

a) At low frequencies current follows the path of least resistance

b) At high-frequencies current follows the path of least inductance

Illustration provided courtesy: Dr. Howard Johnson
Circuit Return Current Simulation @ F=1 Hz

Circuit Return Current Simulation @ F=100 kHz

Circuit Return Current Simulation @ F=5 GHz

Courtesy of Alexander Perez, Agilent Technologies
Common-Mode and Differential-Mode Currents

Differential-mode
1. Conveys desired information.
2. Does not cause interference as the fields generated oppose each other and cancel out.

Common-mode
1. The major source of cable radiation.
2. Contains no useful information.
3. Has no useful purpose.
4. Causes a system (traces, cables, etc.) to radiate as a monopole antenna.

\[
\text{Differential-mode current} \quad I_{\text{total}} = \frac{I_1 - I_2}{2}
\]

\[
\text{Common-mode current} \quad I_{\text{total}} = \frac{I_1 + I_2}{2}
\]
Summary on How EMI Is Developed Within the PCB

1. Current transients are created by the production of high frequency periodic signals injected into the power and return distribution network.
2. An RF voltage drop develops across any impedance within a transmission line.
3. Common-mode RF currents are created by this RF voltage drop on unbalanced RF current return path.
4. Radiated emissions, created by these common-mode RF currents, are observed on internal antenna structures by virtue of poor RF ground loop or return path control.
5. When any time-variant current is injected into a trace, magnetic flux is developed, which in turn creates an electric field. The combination of electric and magnetic fields create a propagating plane wave.
6. Lack of a proper RF current return path exacerbates EMI.
Basic EMC Suppression and Grounding Concepts
**Different Types of Grounds**

- Signal Ground
- Common Ground
- Analog Ground
- Digital Ground
- Safety Ground
- Noisy Ground
- Quiet Ground
- Earth Ground
- Hardware Ground
- Single-point Ground
- Multi-point Ground
- Shield Ground

*What about: RF Ground?*

Often a ground reference may serve multiple needs, each with a different application.
**Defining “Ground”**

**Power/safety ground**
- Intended (neutral) and unintended (safety ground, generally the green wire)
- 50/60/400 Hz

**Lightning ground**
- A controlled path for lightning to reach the earth through a rod or metallic structure
- Generally a 1 MHz event and up to 100 kAmps per millisecond
- Requires a high quality low ground resistance and inductance

**Circuit/signal ground**
- Provides a return path for intended signal flow and for AC/DC power return; mA to Amps
- Requires a minimum low impedance path
- Generally implemented as a ground plane or grids within a printed circuit board
Defining “Ground” (continued)

EMI ground
• Provides a controlled path for RF currents; DC to daylight, μA to Amps
• Requires a minimum ground impedance

ESD ground
• Provides a controlled path for ESD currents
• 0.7-3 ns rise times, 100-300 MHz, 10-50 Amps

RF ground
• Provides an RF return path for flux to return to its source
• Covers the entire frequency spectrum
• Requires minimum impedance for maximum current/flux flow
A ground system topology is determined by
- Signal characteristics
- System dimensions
- System-specific separation and isolation requirements
- Electrical safety requirements

Primary ground system topologies includes
- A “floating” system
- Single-point (“star) ground (SPG)
- Multi-point ground
- Hybrid ground
Three Primary Grounding Methodologies

Single-Point Grounding: Series and Parallel
Multi-Point

SINGLE-POINT: SERIES CONNECTION

SINGLE-POINT: PARALLEL CONNECTION

MULTI-POINT GROUNDING CONNECTIONS
Single-Point: Best for use when signals are below 1 MHz.
• Most sensitive circuit returns should be connected closest to the final equipotential point.
• Provides for greatest amount of loop currents to flow.
• May be used between 1 and 10 MHz if longest conductor is $< \lambda/20$ of a wavelength of highest frequency generated in the system.
• Divided into two type: series and parallel.

Multi-Point: Preferred for frequencies above 1 MHz.
• Minimized loop currents and ground impedance of the planes. A good low inductance ground is necessary for high-frequency digital logic circuits. Ground plane(s) provides a low inductance ground return for RF currents.
• Lead inductance must be kept extremely short.
• Provides for maximum EMI suppression at the PCB level.

Hybrid: For mixed technology products.
• A combination of both single-point and multi-point grounding in the same system
Resonance in a Multi-Point Ground

Printed circuit board.

Inductance in the power planes

Internal power plane capacitance

Eddy currents

V<sub>cm</sub> produced by eddy currents across impedance (Z) from mounting post.

Mounting posts

Mounting plate or chassis

LC resonance in mounting posts

APPLICATION MODEL OF MULTIPOINT GROUNDING

V<sub>cm</sub> is reduced by the mounting posts (ground stitch locations).
Resonance is thus controlled, along with enhanced RF suppression.

ELECTROMAGNETIC MODEL OF MULTI-POINT GROUNDING

Z<sub>B</sub>
RF Current Density Distribution

\[ I(d) = \frac{I_0}{\pi H} \cdot \frac{1}{1 + \left(\frac{D}{H}\right)^2} \]

where
- \( I(d) \) = signal current density, (A/inch or A/cm)
- \( I_0 \) = total current (A)
- \( H \) = height of the trace above the ground plane (in. or cm)
- \( D \) = perpendicular distance from the center line of the trace (in. or cm)
Ground Slots Created with Through-Hole Components

Through-holes (multiple holes in one straight line) creates a slot in the ground plane. Return current must travel around the slot.

Through-holes (multiple holes spaced apart) Optimal method of routing traces if through-hole components must be used.

Signal trace

RF return current

I.C.                  Ground Plane

Signal trace

Return current in ground plane

E = L \frac{dl}{dT} = plane radiation

Equivalent circuit showing inductance in the return path. This inductance is approximately 1 nH/cm.
Functional Partitioning

- Adapter cards
- Slow speed I/O interconnects
- Support logic
- Video
- Audio
- Analog processing
- CPU and clock logic
- Power supply
- Memory section

Slow speed I/O
- CPU and clock logic
- Memory section
- Power supply
- Video
- Audio
- Adapter cards
- Support logic
- Memory section
- Analog processing
- Slow speed I/O interconnects
- Video
- Audio
Bypassing and Decoupling
(Power Distribution Networks)
The Need for Optimal Power Distribution

- Provides a stable voltage reference between components to ensure functional operation
- Distribute optimal power to all logic devices to minimize planar bounce

Key items of concern
Use low impedance connections between logic gates:
- The impedance between power pins on gates should be just as low as the impedance between the return pins on the same device
- A low impedance path must always be provided between power and return

Charging current for capacitor C flows through the inductance of the power distribution network
Power Distribution Networks as Transmission Lines

Power distribution networks can be represented as a two conductor transmission line with a defined characteristic impedance and propagation delay.

Ideal Power Distribution Network – Multiple Loads

Real-Life Power Distribution Network – Multiple Loads
Primary Requirements for Enhanced Power Distribution

The amplitude of power supply transients are directly proportional to the characteristic impedance of the power distribution system, $Z_0$:

**To reduce $Z_0$**

- Reduce inductance
- Increase capacitance

\[ Z_0 = \sqrt{\frac{L_0}{C_0}} = \frac{V(x)}{I(x)} \]

**Both are achieved by**

- Reduction of loop area between conductors (less inductance)
- Placing conductors as close together as possible (greater capacitance)
- Increase of conductors’ width (less inductance and greater capacitance, with respect to another conductor)
Defining Capacitor Usage

Capacitors are used for one of three primary functions.

**Bulk**
Used to maintain constant DC voltage and current levels on a global basis due to IR drops within the power distribution network, and to recharge the distribution network (i.e., planes) cause by $dl/dt$ consumption from components (typically 1-100 $\mu$F).

**Bypassing**
Diverts or steers RF currents from one location to another. Shunts unwanted common-mode RF currents from components or cables from entering susceptible areas in addition to providing other functions of filtering (bandwidth limited).

**Decoupling**
Provides a localized source of DC power, and are particularly useful in reducing peak current surges propagated across the board. Prevents RF currents from being injected into the power distribution network during digital component edge transitions.

- Switching transient capacitance (0.01 $\mu$F) – Used to supply short-term energy demands of the silicon during switching states.
- Line charging capacitance (0.1 $\mu$F) – Used to charge capacitive transmission lines as well as supplying current necessary for the driver.
Effective Range of Decoupling Systems and Target Impedance

(Artwork provided courtesy – Ansoft Corporation)
Calculating Power and Return Plane Capacitance

Capacitance of the power and ground planes is defined by:

\[ C_{pp} = k \frac{\varepsilon_r A}{D} \]

where
- \( C_{pp} \) = capacitance of parallel plates (pF)
- \( \varepsilon_r \) = dielectric constant of the board material
- \( A \) = area between the parallel plates (square inches or cm)
- \( D \) = distance spacing between the plates (inches or cm)
- \( k \) = conversion constant (0.2249 for inches, 0.884 for cm)
Capacitors and Resonance

Self-resonant frequency
Through-hole capacitors

Impedance (Ohms)

1/4 inch or 0.64 cm leads – 15 nH

Self Resonant Frequency - SMT Capacitors

Impedance (Ohms)

Impedance versus Frequency graph for SMT capacitors, showing the self resonant frequency at different capacitance values (100 pF, 0.001 μF, 0.01 μF, and 0.1 μF).

Frequency (MHz)

Effects of Capacitors in Parallel – Different Values

PARALLEL DECOUPLING CAPACITORS

MAGNITUDE \times 10^{-1}

FREQUENCY \times 10^7 Hz


Effects of Capacitors in Parallel – Same Capacitor Values

How to calculate number of capacitors with the same capacitive value in parallel:

\[ C_{\text{total}} = n \times C \]
\[ L_{\text{total}} = \frac{L}{n} \]
\[ ESR_{\text{total}} = \frac{ESR}{n} \]
\[ |Z| = \sqrt{\left( \frac{ESR}{n} \right)^2 + \left( \frac{\omega ESL}{n} - \frac{1}{\omega nC} \right)^2} \]

(Plot provided courtesy AVX Corp.)
**Power and Ground Plane Capacitance**

Power and ground plane configuration
(Bare board configuration)

\[ |Z| = \frac{1}{2 \pi f C} \]

Discrete decoupling capacitor

\[ |Z| = \frac{1}{2 \pi f C} \quad (f < f_s) \]

Bare board without decoupling

Decoupling

C_{plane}  L_{board}  C_{board}  C_{cap}
Conflicting Rules for PCB Decoupling

Use small-valued capacitors for high-frequency decoupling

Use 0.01 μF for local decoupling

Locate capacitors near the power pins of active devices

Use capacitors with a low ESR!

Avoid capacitors with a low ESR

Locate capacitors near the ground pins of active devices

Locate of the decoupling capacitors is not relevant

Use 0.001 μF for local decoupling

Never put traces on decoupling capacitors

Use the largest valued capacitors you can find in a given package size

Local decouping capacitors should have a range of values from 100 pf to 1 μF

List created by Todd Hubing
Interconnects and I/O
Partitioning

Functional Subsystems
A group of components along with their respective support circuitry performing a common function.

Quiet Areas
Sections physically isolated from other functional areas to prevent noise sources from corrupting susceptible circuits in the quiet zone.

Internal Radiated Noise Coupling
Radiated RF coupling may occur between different functional subsections. To prevent this coupling, a fence or shield barrier may be required. A fence is a metal barrier secured to the ground plane(s) at intervals appropriate for the highest frequencies anticipated (at $\lambda/20$ wavelength intervals) and tall enough in height to prevent direct line RF radiated field coupling.
Isolation (Moating)

- Best location for ground connection
- Isolation transformer
- Moat
- Data line filter (common-mode choke)
- I/O connector

Absence of voltage and ground planes (to minimize coupling capacitance across the DLF)

Ground trace, if required, 3x wider than power trace
- Ferrite bead-on-lead to bridge power (only) into the moated area. Do not use an inductor
- Optional decoupling capacitor, usually necessary to ground, not across the moat
Isolation transformer or optical isolators

Moat

Data line filter

Shield-shell ground connection to chassis

I/O connector

Absence of voltage and ground planes

Non-isolated power and shield grounds to chassis

Decoupling capacitors

Ferrite filter (with fuse)

Power

Ground
**Bridging**

Connection to chassis ground

Moat

I/O connector

Bridge in moat

Location of optional grounds to chassis

Ferrite bead-on-lead for optional power, if required, over a separate moat for power plane. (dotted line).
Image Plane or Moat Violation

Moat violation

Signal Trace

Large loop area allows for common-mode RF energy to exist due to lack of an image plane along the entire trace route.

Correct use of moating